REMARKS

Prior to this Response, an Office Action was issued, mailed January 3, 2003.

In the Office Action, claims 5-7 and 9 were rejected.

In this Response, claim 5 has been amended.

The amendment to claim 5 constitutes a bona fide attempt by the applicant to advance the prosecution of the application and obtain allowance, and is in no way meant to acquiesce to the substance of the Examiner's rejection.

In this Response, claims 10-17 are added. No new subject matter is added.

Claims 5-7 and 9-17 are pending in the present application. Reconsideration is requested. In addition to the referenced amendments, the Applicant makes the following remarks regarding individual issues.

Claim Rejections – 35 USC § 103

Claims 5-7 and 9 stand rejected under 35 U.S.C 103(a) as being unpatentable over Subramanian et al. (US Patent No. 5,668,021, hereafter the '021 reference) in view of applicant's Admitted Prior Art (AAPA). Applicant respectfully traverses this rejection. Claim 5 is amended to more clearly state recited limitations.

In response to sections 2 and 3 of the Office action, the applicant respectfully disagrees that '021 discloses an impurity implantation region of the first sector comprising a depletion channel of the second conductivity type occupying a surface region of the semiconductor substrate. The Examiner stated that Fig. 7 of Subramanian et al. depicts the top of region 24 being in direct contact with the surface of the substrate and that buried junction 24 has a surface region, not spaced away from the surface of the substrate, as a depletion channel.

The references, however, must be considered as a whole. *Hodosh v. Block Drug Co., Inc.*, 786 F.2d 1136, 1143 n.5, 229 USPQ 182, 187 n.5 (Fed. Cir. 1986). A prior art reference must be considered in its entirety, i.e., as a whole, including portions that would lead away from the claimed invention. *W.L. Gore & Associates, Inc. v. Garlock, Inc.* 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983), *cert. denied,* 469 U.S. 851 (1984). By considering only FIG. 7 of the '021 reference, the Examiner fails to take into account the other relevant teachings of the '021 reference regarding the "buried junction 24."

The '021 reference warns that for simplicity and clarity of illustration, the accompanying figures are not necessarily drawn to scale, further indicating that care must be taken when considering FIG. 7 (column 2, lines 34-36). Proportions of features in a drawing

are not evidence of actual proportions when drawings are not to scale. MPEP 2125. The description of the article pictured can be relied on, in combination with the drawings, for what they would reasonably teach one of ordinary skill in the art. *In re Wright*, 569 F.2d 1124, 193 USPQ 332 (CCPA 1977).

As previously stated, the '021 reference teaches that the peak dopant concentration of buried junction region 24 is placed, not at the surface, but *just below* the surface of substrate 10 ('021, column 3, lines 65-66, emphasis added). Since the buried junction region 24 is egg-shaped (FIG. 7), the topmost portion of buried junction region 24 must also lie just below the surface of substrate 10. According to Random House Webster's College Dictionary, 2000 ed., the word "just" can mean "*exactly*" or "*by a narrow margin, barely.*" In either case, regardless of whether the term "just below" in the '021 reference is deemed to mean "exactly below" or "barely below", the surface of the buried junction region 24 is nevertheless *below* the surface of semiconductor substrate 10. This is in keeping with the normal meaning of the word "buried."

The Examiner gives the term "buried" a meaning that is completely opposite to what one of ordinary skill in the art would expect, especially when the '021 reference goes to great lengths to distinguish between "buried junction regions" and "surface channel regions" (column 1, lines 27-36; column 2, lines 8-13; column 2, lines 46-48; column 5, lines 63-65). For example, surface channel regions 50 and 52 of FIG. 7 are on either side of the buried junction region 24 (column 5, lines 63-65). Because '021 explicitly states that regions 50 and 52 are surface channel regions, a "buried junction region 24" would not suggest to one of ordinary skill in the art that it occupies a surface region of the semiconductor substrate, as recited in claim 5.

In sum, it does not matter how close (or, in the Examiner's words, "not spaced away from") Subramanian FIG. 7 shows the surface of buried junction region 24 to be to the surface of semiconductor substrate 10. When considered as a whole, including the portions that lead away from the claimed invention, the '021 reference indicates to one of ordinary skill in the art that the surface of buried junction region 24 is *below* the surface of semiconductor substrate 10 (emphasis added). The entire "buried junction region 24" is consequently *completely covered* by the surface of the substrate 10, making it impossible for the buried junction region 24 to occupy a surface region of the semiconductor substrate, as recited in claim 5 (emphasis added).

Furthermore, if the "buried junction region 24" actually occupied a surface channel region as the Examiner suggests, then the entire device would not function as Subramanian

intended. The '021 reference teaches that both buried channel devices and surface channel devices each have their own unique set of advantages (column 1, lines 28-43). For example, buried channel devices have high current mobility, but short channel effects are aggravated by large depletion regions in buried channel devices (column 1, lines 33-35). In contrast, surface channel devices are more resistant to short channel effects such as drain induced barrier lowering and electrical punchthrough than buried channel devices (column 1, lines 35-39). Subramanian explicitly teaches that the device pictured in FIG. 7 has both surface channel regions and a buried junction region, *combining the advantages of both surface channel devices and buried channel devices*. (column 2, lines 5-15, emphasis added).

If, in fact, the "buried channel region 24" of FIG. 7 does occupy a surface region of the substrate, then the entire channel region (buried channel region 24 and surface channel regions 50, 52) is a surface channel, and Subramanian's goal of combining the advantages of both buried channel devices and surface channel devices is not achieved. Thus, one of ordinary skill in the art, considering the '021 reference as a whole, would not conclude that "buried junction region 24" occupied a surface region of the semiconductor substrate. Doing so is contrary to the explicit teachings of the '021 reference.

Because the combination of AAPA and the '021 reference fail to teach or disclose all the recited structural limitations of claim 5, a *prima facie* case of obviousness has not been established.

With regard to section 5 of the previous action, the Examiner has misstated the applicant's argument. The applicant is not arguing, as stated by the Examiner in section 5, that "AAPA is not prior art..." The applicant actually objected to the use of portions of the applicant's own disclosure regarding the applicant's own perceptions about the AAPA as being, in itself, AAPA. Specifically, on page 4, lines 16-17 of the Office Action mailed on July 15, 2002, the Examiner stated that "[t]he combination is motivated by the teachings of AAPA who point out the need for an improved pull-up transistor." Strictly speaking, the AAPA in this case is FIG. 1, FIG. 2, FIG. 3, and FIG. 4 of the applicant's disclosure, nothing more.

The need for the pull-up transistor found in the applicant's disclosure is applicant's teaching, not that of the AAPA. The applicant pointed out disadvantages and drawbacks related to the AAPA. The disadvantages of the prior art (what the prior art lacks) cannot be said to teach, either explicitly or implicitly, the combination of '021 and AAPA. The Examiner suggests that the disadvantages of the AAPA would be apparent to one of ordinary skill in the art, but the level of skill in the art cannot be relied upon to provide the suggestion

to combine references. *Al-Site Corp. v. VSI Int'l Inc.*, 174 F.3d 1308, 50 USPQ2d 1161 (Fed. Cir. 1999).

The applicant respectfully submits that the Examiner is reciting combinations and advantages as a result of an impermissible benefit of hindsight afforded by the present patent application. Prior art references in combination do not make an invention obvious unless something in the prior art suggests a motivation for combining their teachings. It is not enough that the Examiner cite advantages; the Examiner should point to where these advantages are mentioned in the cited prior art references — absent the present teachings of applicant.

In summary, the '021 reference and the AAPA do not teach or suggest all the claim limitations of claim 5. Even if they do — which applicant disputes — the '021 reference and the AAPA, when fairly read without the benefit of the applicant's specification, do not present a teaching or a motivation to combine reference teachings.

Accordingly, applicant submits that claim 5 is patentable over the combination of the '021 reference and the AAPA. Likewise, it follows that dependent claims 6-7 and 9 also are patentable, at least for reason of being dependent upon a patentable base claim.

NEW CLAIMS

Claims 10-17 are added, no new subject matter is present.

Independent claim 10 is similar to amended claim 5, and recites a first sector. But new claim 10 also recites an impurity implantation region with impurities of a second conductivity type formed on the semiconductor substrate and with a lateral extent coextensive with the first sector. Claim 10 also recites that the impurity implantation region comprises a first surface channel region that functions as a depletion channel and that occupies the entire top surface of the semiconductor substrate within the first sector.

Conversely, in FIG. 7 of Subramanian, an entire top surface of the semiconductor substrate 10 coextensive with the first sector is not occupied by the buried junction region 24.

New claims 11-13 are substantially similar to claims 6, 7, and 9, respectively.

Independent claim 14 contains the limitations of independent claim 10 but additionally recites that the first surface region has a top surface and a bottom surface with the top surface having a greater extent than the bottom surface.

Conversely, in FIG. 7 of Subramanian, the top surface is not longer than the bottom surface of the buried junction region 24.

New claims 15-17 are substantially similar to claims 6, 7, and 9, respectively.

Because the combination of AAPA and Subramanian does not disclose all the limitations of claim 10 or 14, those claims are not *prima facie* obvious with respect to that prior art. The claims that depend from claim 10 or 14 are also allowable for at least that reason.

CONCLUSION

It is believed that claims 5-7 and 10-17 are in condition for allowance and such is respectfully requested.

The Examiner is encouraged to telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

Respectfully submitted,
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